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10/726,470	12/02/2003	Shridhar Mukund	ADAPP223	5856

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,470	MUKUND ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 22 January 2008, PROSECUTION IS HEREBY REOPENED. New ground of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Narayan et al. (U.S. Patent No. 5,822,559), herein referred to as Narayan et al.'559.

Referring to claim 1, Narayan et al.'559 discloses, as claimed, a networking application processor (see Fig. 2), comprising: an input socket configured to receive data packets (the input data from I/O module of the system intended to be used); a memory (such as main memory of the Narayan et al.'559's system or instruction cache 204, see Fig. 2) for storing instructions (any memory can be used for storing instructions); circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access an operand from a memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2 or the register between pipeline stages inherent in any pipelined processor); an arithmetic logic unit (ALU) (inside function units 212A-212D, see Fig. 2); and circuitry for aligning operands (operand steering section; see fig.

29) to be processed by the ALU, the circuitry for aligning operands causing the operand to be aligned by a lowest significant bit (see col. 115, lines 7-10;

> *note that operands must be aligned by a least significant bit in order to perform calculations. For example, if two numbers are to be added [56 and 1985, or 111000 and 11111000001], the numbers inherently must be aligned by the least significant digit.*

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       111000   (56)
+ 11111000001 (1985)
  11111111001 (2041)
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> *Any other method of alignment prohibits correct addition),*

wherein the circuitry for aligning the operand supplies an extension (in the situation when the real operand size is less than the size to be processed) to the operand to allow the ALU to process different size operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

Referring to claim 14, Narayan et al.'559 discloses, as claimed, a processor capable of processing a data packet associated with a processing stage of a pipeline of processors (see col. 1, lines 15-20; each pipeline stage does processing and therefore any pipelined processor contains a "pipeline of processors") the processor comprising: a data random access memory (RAM) (such as the main memory of the Narayan et al.'559's system) configured to enable access to data structures; instruction fetch and decode circuitry (comprising such as early decode units 207A-207D and MROM and anything else relating to decoding, see Fig. 2) configured to interpret instructions to be executed by an arithmetic logic unit (ALU) (function units 212A-212D, see Fig. 2), the

instruction fetch and decode circuitry including, a read only memory (ROM) (such as portion of the MROM of the Narayan et al.'559's system comprising the microcode sequences; such as the exception routine described on col. 145, lines 43-56), the ROM configured to store code common to each processing stage associated with a pipeline of processors; a code RAM (The Section of MROM unit 209 storing MROM instructions, see Fig. 2; col. 14, lines 27-35 regarding storing MROM instructions), the code RAM configured to download code specific to the processing stage; and instruction decode circuitry (comprising such as decode units 208A-208D, see Fig. 2) configured to recognize operating instructions; execute and write back circuitry (comprising function units 212A-212D, see Fig. 2) configured to set up operands to be processed by the ALU, the execute and write back circuitry including, internal registers (inside register file 218, see Fig. 2) for defining a first and a second operand; an arithmetic logic unit (function units 212A-212D, see Fig. 2) for processing the first and second operands; and align function circuitry (instruction alignment unit 206, see Fig. 2) for aligning the first and the second operands to be processed by the ALU, the align function circuitry causing the first and the second operands to be aligned by a lowest significant bit, wherein the align function circuitry supplies an extension (in the situation when the real operand size is less than the size to be processed) to the each of the operands to allow the ALU to transparently process different size operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

As to claim 2, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the instructions have a width of 96 bits (see the instruction

set in Fig. 1 when it comprises 12 bytes=96 bits), and wherein the single cycle access enables the data to be addressed and operated on in a single cycle in a single clock cycle without being placed into a register (see col. 10, last paragraph).

Note that if an instruction is fetched, the data contained within that instruction is addressed (with a program counter) and operated on (read from memory). The definition of the word "operate" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "to perform a function; work". Under this definition, a read (fetch) from memory is reasonably considered to be an operation.

As to claims 3 and 16, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the different size operands are selected from the group consisting of 8 bit operands, 16 bit operands, and 32 bit operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

As to claim 4, Narayan et al.'559 also discloses: the networking application processor of claim 1, further including: an output socket for transmitting processed data; and a 64 bit bus (see such as 64-bit input bus to decode unit 0-3, see Fig. 25) connecting the input socket and the output socket.

As to claims 5 and 15, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the extension to the operand fills each higher bit with a value (such as 0 for each higher bit for the unsigned operands).

As to claim 6, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the operand is selected from the group consisting of a source operand, a destination operand, an immediate operand, and an internal register operand (see col. 2, lines 5-23, and Fig. 1, regarding the instruction set format including source operand, a destination operand, an immediate operand).

As to claim 17, Narayan et al.'559 also discloses: the processor of claim 14, wherein the operating instructions wherein the operating instructions are formatted as 96 bit instructions (see the instruction set 100 in Fig. 1 when it comprises 12 bytes=96 bits), each of the 96 bit instructions including a single return bit (the bit such as end of file or record in the instruction set 100 in Fig. 1).

As to claim 18, Narayan et al.'559 also discloses: the processor of claim 14, wherein the processor is configured as a two stage pipeline for pipelining an instruction fetch and decode operation (using prefetch/predecode unit 202; and decode units 208A-208D, see Fig. 2) and an execute and write back operation (see Col. 144, lines 45-65, regarding write back operations).

As to claim 19, Narayan et al.'559 also discloses: the processor of claim 14, wherein the operating instructions include microcode configured to predict a likely direction for a branch instruction (using branch prediction unit 220, see Fig. 2).

As to claim 20, Narayan et al.'559 also discloses: the processor of claim 19, wherein no operation (NOP's) instructions are included (see such as col. 139, lines 4-5, regarding some of the instructions may be NOOP), the NOP's configured block an invalidated pre-fetched instruction.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al.'559.

Referring to claim 7, Narayan et al.'559 discloses, as claimed, a processor (see Fig. 2), comprising: an input socket (the input data from I/O module of the system intended to be used) configured to receive data packets; a memory (such as main memory of the Narayan et al.'559's system or instruction cache 204, see Fig. 2) for storing instructions; circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access from a memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2); and an arithmetic logic unit (ALU) (inside function units 212A-212D, see Fig. 2), the ALU configured to receive a first and a second operand (operand A and operand B, see Fig. 33); the second operand being specified from an internal register (REGF, see Fig. 33).

Narayan et al.'559 discloses the claimed invention except for explicitly showing the first operand having a mask enabling the ALU to process a non-masked segment of the first operand.

However, Narayan et al.'559 shows using masks to select bytes before sending to the register file for the further use (see Col. 144, lines 59-60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Narayan et al.'559's system to comprise the first operand having a mask enabling the ALU to process a non-masked segment of the first operand,

as also taught by Narayan et al.'559, in order to facilitate selecting the useful bytes to be processed and saving the processing time in the Narayan et al.'559's system.

As to claim 8, Narayan et al.'559 also discloses: the instructions have a width of 96 bits (see the instruction set in Fig. 1 when it comprises 12 bytes=96 bits) as set forth in claim 2 above.

As to claim 9, Narayan et al.'559 also discloses: the processor of claim 7, wherein each of the instructions include a loadback feature enables random accesses to one of a source indirect register or a destination indirect register through indirect addressing (see Fig. 1 and col. 2, lines 5-22 regarding such as adding the displacement value to the content of a register to form a memory location).

As to claim 10, Narayan et al.'559 also discloses: the processor of claim 7, wherein the mask is associated with an immediate value (see Fig. 1, the instruction set comprising the immediate field) of the first operand.

As to claim 11, Narayan et al.'559 also discloses: first and the second operands are associated with a size selected from the group consisting of 8 bit operands, 16 bit operands, and 32 bit operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits) as set forth in claim 3 above.

As to claim 12, Narayan et al.'559 also discloses: the processor of claim 7, wherein the first operand is selected from the group consisting of a source operand, a destination operand, an immediate operand, and an internal register operand (see col. 2, lines 5-23, and Fig. 1, regarding the instruction set format including source operand, a destination operand, an immediate operand) as set forth in claim 6 above.

As to claim 13, Narayan et al.'559 also discloses: the method of claim 7, wherein the memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2) is a static random access memory (SRAM).

Response to Arguments

5. Applicant's arguments filed 21 September 2006 have been fully considered but they are not persuasive.

6. Applicant states:

> 1. Narayan does not teach a single cycle access or circuitry, for aligning operands to be processed by the ALU~ the circuitry for aligning operands causing the operands to be aligned by a lowest significant bit~ wherein the circuitry for aligning the operands supplies an extension to the operands to allow the ALU to process different size operands.

Examiner disagrees. As stated in the previous Office Action, the specification makes no specific definition of the term "single cycle access". Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is unreasonable to limit the term "single cycle access" to only include an access in which "data is addressed and operated on in a single clock cycle". The specification merely points that the apparatus can work in that fashion. Examiner suggest adding this limitation into the claim for clarity instead of attempting to assign a specific definition to a broad term. Additionally, any pipelined processor inherently accesses memory in one clock cycle from the registers between pipeline stages. Since there are no

additional limitations on which memory is accessed in one clock cycle, all pipelined processors fall within this limitation.

7. Applicant states:

> 1. Narayan does not teach circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access from memory

Examiner disagrees. As stated above, the term "single cycle access" is extremely broad. Additionally, The limitations only requires that the circuitry be able to access data and perform a single cycle access from a memory location. "While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function." In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). The limitation merely recites circuitry that is configured to read a type of data. Any processor is able to read data, no matter what the data is associated with.

8. All remaining arguments been considered but are moot in view of the new ground(s) of rejection. A detailed explanation is given above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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